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**IMPROVED PARASITIC SPEED CONTROLLERS
FOR SPACE POWER SYSTEMS**

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ABSTRACT

The dynamic space power systems under investigation use parasitic speed controllers to regulate the rotational speed and frequency of the alternators. The speed controller regulates speed by applying an increasing parasitic load whenever the useful load is decreased and speed increases. The performance of present controllers employing phase-controlled loading have met major design goals, and the controllers have operated successfully in various systems for many thousands of hours; however, these controllers have performance characteristics which could be improved such as the reduction or elimination of (1) distortion of the line voltage, (2) high neutral currents, (3) additional volt-ampere loading on the alternator, (4) unbalanced loading of the three phases, and (5) nonlinearity of the control characteristic.

Modifications of control logic are being investigated as ways to improve these characteristics. A modification being investigated is an increase in the number of stages for a given load range with each stage controlling a reduced amount of parasitic load. Other modifications include the addition of active nonlinear networks and power feedback networks. A design employing only digital circuitry is also being investigated. With this approach, a discrete amount of parasitic load would be varied for a discrete change in frequency. The paper discusses and evaluates these design concepts.

The largest improvement in the electrical performance characteristics of these power systems is obtained by using an all-digital speed controller. However, the digital speed controller requires the use of a relatively large number of parasitic load elements. When only a few load elements are available, significant improvements in the performance characteristics can be obtained by using suitably modified existing speed controllers.

THE DYNAMIC SPACE POWER systems under investigation at the Lewis Research Center are self-contained systems which operate on either a Rankine or a Brayton thermodynamic cycle. The energy sources of interest for these systems are solar energy, radioisotopes, and nuclear reactors. These sources produce a constant power output. The electrical power source is a turbine-driven alternator which has a constant power input. Therefore, the alternator produces a nearly constant output power. The power that is not consumed by the useful (vehicle) load must be dissipated in order to obtain a torque balance on the alternator. The parasitic speed controller accomplishes this function by sensing a change in the speed of the alternator and by adjusting the parasitic load until this torque balance is obtained. The speed varies inversely with the useful load applied to the alternator.

Two methods of varying the parasitic load are considered in this paper: the phase-controlled method and the all-digital method using zero-voltage switching of the loads. In the phase-controlled method saturable reactors or silicon controlled rectifiers (SCR's) are used as the load-control elements. They control the effective value of the voltage applied to the load resistors. In the digital method SCR's are also used as the load-control elements. With this method the number of multiple loads applied to the alternator is varied. Each load is either fully conducting or off. This method has not been demonstrated in a developmental system.

Parasitic speed controllers employing phase-controlled loading are used in these space power systems: the SNAP-8 system, the 400-hertz Brayton system, and the 1200-hertz Brayton system. Electrical performance characteristics of these systems are presented in Refs. 1 to 5. This paper discusses and evaluates design concepts for improving the electrical performance characteristics of these systems. Modifications which should minimize some of the undesirable characteristics inherent in the phase-controlled loading method are described. A speed controller design using all-digital circuitry is also discussed. It is being considered since it avoids many of the undesirable characteristics of the phase-controlled method. However, it has new potential problems which are under investigation. Some of these ideas are to be incorporated in future speed controller designs.

PHASE-CONTROLLED LOADING SPEED CONTROLLER

BASIC CHARACTERISTICS - In the 1200-hertz Brayton system, an alternator, a turbine, and a compressor are mounted on a common shaft (3)*. The 400-hertz Brayton system uses a turboalternator and a turbocompressor (2). The SNAP-8 system uses a turboalternator (5). The basic configuration of the electrical system is the same for any of these systems. A diagram of the electrical system is given in Fig. 1a. The output voltage of the alternator is three-phase, four-wire.

The ideal load sharing of a parasitically loaded alternator is illustrated in Fig. 1b. This characteristic is for a proportional controller. An integral type of controller which has zero steady-state frequency error can also be designed (6), but it has not been demonstrated in a developmental system. The parasitic load adds to the useful load so that the total alternator load is a constant. The controller senses the frequency of the alternator voltage and applies the parasitic load required to complement a particular useful load. The frequency range is established by adjusting the controller for a minimum frequency deviation consistent with system stability.

Figure 2 is a functional block diagram of the controller. The frequency discriminator measures the frequency deviation. The output of the discriminator is amplified by the power amplifier. This amplifier controls the magnitude of the current in the parasitic load resistors. Ideally, the load currents for each phase are equal. The waveshape of the phase-controlled current is illustrated in Fig. 3. Varying the firing angle changes the effective value of the load current. Varying the firing angle also has the effect of changing the phase angle between the applied voltage and the fundamental component of the nonsinusoidal current (7). The current fundamental lags the voltage as in an inductive circuit. The result is that the alternator must be able to supply an inductive load in addition to the usual design requirement, that is, the apparent-power requirement is larger. Since the internal impedance of an alternator is not zero, the nonsinusoidal current causes distortion in the alternator output voltage.

*Numbers in parentheses designate References at end of paper.

Parasitic speed controllers employing phase-controlled loading actually have a nonlinear load-frequency characteristic (8). Figure 4 illustrates this characteristic which holds for a constant distortion-free line voltage. Phase-controlled loading also generates appreciable neutral currents. Investigations have shown that the maximum value of neutral current is equal to the parasitic load current at maximum conduction angle.

The characteristics inherent in the use of phase-controlled loading are (1) the additional volt-ampere loading on the alternator, (2) distortion of the line voltage, and (3) the generation of neutral current. The characteristics which depend only upon circuit design are (1) the possible unbalanced loading of the three phases and (2) the nonlinearity of the control characteristic.

REDUCTION OF APPARENT-POWER REQUIREMENT, CURRENT DISTORTION, AND NEUTRAL CURRENT - Gilbert (7) has shown how the use of multiple parasitic loads sequentially actuated lessens the undesirable effects of an additional apparent-power requirement and distortion of the alternator current. The 400-hertz Brayton and the 1200-hertz Brayton speed controllers employ three sequentially-actuated loads, whereas the SNAP-8 system employs only one parasitic load. Two of the three loads in the Brayton systems operate over the normal control range. The third load serves two functions:

1. It provides speed control capability when the alternator develops more than its rated power as may occur during cold startup.
2. It serves as a redundant load should one of the first two loads fail.

An improvement being investigated is a further division of loads. The results of Gilbert indicate that by using four active loads, the additional apparent-power requirement for a 0.8-lagging-power-factor useful load is reduced from 3.0 percent to 1.3 percent. For the same load condition, the maximum total harmonic distortion of the alternator current is reduced from 18 percent to 9.5 percent. Less current distortion gives less voltage distortion. The voltage regulation in these systems depends to some extent on the magnitude of the voltage distortion (2,3,4). Therefore, an improvement in the voltage regulation should occur. The degree of the improvement depends on the type of voltage regulator used in the system.

As previously indicated, by reducing the full-conduction current for a load, the maximum value of the neutral current is decreased. Doubling the number of active loads then reduces the maximum value of the neutral current by about 30 percent.

The results of Ref. 7 indicate that the amount of improvement for each load division decreases rapidly with increasing number of loads. The number of loads in a given system may be limited by other factors. Certain system considerations, such as size and weight, may determine the maximum number of load divisions.

Perz (9) gives experimental results which indicate that further improvement in total harmonic current distortion may not occur upon further division of loads. Because of design limitations, the firing circuits require a minimum firing angle to turn on the SCR's. As a consequence, the load is not on for the full 180 degrees of the sine wave and the total harmonic distortion of the current does not go to zero. This effect is cumulative and causes an experimental distortion greater than the theoretical maximum. Therefore, in order to obtain the most improvement in the above characteristics, the firing angle must be minimized.

PARASITIC LOAD UNBALANCE - A parasitic load unbalance between phases of about 5 percent of the useful alternator output power has been obtained experimentally. The unbalance, if severe, may cause the alternator armature design temperatures to be exceeded. The unbalance in the parasitic load is a function of the circuit components used. Figure 5a is a characteristic obtained during the initial testing of a speed controller for the 1200-hertz Brayton system. By making certain adjustments and without changing the basic circuit design, characteristics as in Fig. 5b were obtained. The maximum unbalance as shown is about 2 percent of the rated alternator output power.

In the 400-hertz Brayton system a maximum unbalance of about 1.5 percent of the rated alternator power was obtained (2). New circuit designs are being considered which will give a maximum unbalance of less than 1 percent without requiring detailed adjustments.

Feedback circuits are also being considered which allow the application of unbalanced useful loads by automatically ad-

justing the parasitic load to obtain a balanced total alternator load. In power systems which are run at only one power factor, this function can be performed by limiting to a constant (rated) alternator line current. Varying the power factor would cause an effective change in the speed controller gain. Further modifications to the speed controller could be made to accommodate this changing gain and ensure system stability. The power factor of the total alternator load will actually vary over some range. In particular, the phase-controlled load has a power factor which varies with the magnitude of the load (4). The alternator current, therefore, would be limited to the value obtained at the lowest power factor of the total alternator load.

A block diagram of a limiting scheme is shown in Fig. 6. The alternator produces a constant output power and, if the power factor is constant, a constant output current. At rated line current the current limiter produces no output signal. When excess useful load is applied to one phase, the current limiter on that phase generates a signal which causes the parasitic load current to decrease. The alternator line current returns to within a small error of its rated value. This error is determined by design of the current limiter and by the requirement of system stability.

The following discussion illustrates some of the considerations involved in the design of a current limiter. It is assumed that no change in frequency occurs for the application of an unbalanced useful load. Figure 7a is a functional block diagram of the limiter. Assume that initially the useful load current (I_u) is zero. Then the parasitic load current is equal to the rated alternator current, or $I_p = C$. The error signals E_1 and E_2 are also zero. The block diagram in terms of transfer functions is obtained as in Fig. 7b. The current limiter and the speed controller are assumed to be simple lag circuits. The equation for the error E_1 in terms of Laplace transforms is

$$E_1(s) = I_p(s) + I_u(s) - C$$

$$= - \left(\frac{K_L}{1 + \tau_L s} \right) \left(\frac{K_p}{1 + \tau_p s} \right) (E_1 + C + I_u - C)$$

where S is the Laplace operator. This is rewritten as

$$\frac{E_1(S)}{I_u(S)} = \frac{1}{1 + \frac{K_L K_p}{(1 + \tau_L S)(1 + \tau_p S)}}$$

The final value for the error is

$$E_1(S = 0) = \frac{1}{1 + K_L K_p}$$

when I_u is a step input of unity magnitude. Realistic values for τ_L and τ_p are

$$\begin{aligned}\tau_p &= 0.001 \text{ sec} \\ \tau_L &= 0.01 \text{ sec}\end{aligned}$$

Further analysis indicates that if $K_L K_p \leq 2$, then there will be no oscillations in the error E_1 . However, the steady-state error is then

$$E_1(S = 0) = \frac{1}{1 + 2} < 0.34$$

In order to obtain an error less than 0.3 and a nonoscillatory response, compensating networks will be included in the final design.

LINEARIZATION OF THE LOADING CHARACTERISTICS - As was discussed previously, the parasitic load-frequency characteristic in present controllers is nonlinear. A typical characteristic obtained in system testing is shown in Fig. 8. For a given control range, the slope of the load-frequency characteristic (or the gain) at some operating points may be sufficiently large to cause significant parasitic load fluctuations. The fluctuations cause voltage and alternator power fluctuations. In systems where these fluctuations occurred, the control range was extended. Lowering the gain in this fashion eliminated the fluctuations (2,3).

Figure 9a is a block diagram illustrating an approach to linearize the control characteristic. An electronic multiplier is inserted in the feedback loops of a high gain amplifier and the firing circuit. The filter is required in order to prevent a high-frequency modulation of the firing angle. The input to the control loop is a linear function of the frequency. The multiplier measures the instantaneous value of power dissipated in the resistor. The filter

averages the output of the multiplier and provides the voltage to be compared with the input to the loop.

A block diagram of this method in terms of Laplace transforms is given in Fig. 9b. The ratio of parasitic load to frequency is

$$\frac{P(S)}{F(S)} = \frac{AK_1}{(1 + \tau_1 S) \left[1 + \frac{AK_1}{(1 + \tau_1 S)} \cdot \frac{K_2 K_3}{(1 + \tau_3 S)} \right]}$$

where S is the Laplace operator. Rewriting,

$$\frac{P(S)}{F(S)} = \frac{AK_1(1 + \tau_3 S)}{(1 + \tau_1 S)(1 + \tau_3 S) + AK_1 K_2 K_3}$$

For a step change in frequency of unit magnitude, the steady-state value of parasitic power is

$$P(S = 0) = \frac{AK_1}{1 + AK_1 K_2 K_3}$$

If the product $AK_1 K_2 K_3 \gg 1$, then

$$P(S = 0) = \frac{1}{K_2 K_3}$$

Now the change in parasitic power is independent of the nonlinear gain K_1 . The gains K_2 and K_3 are selected to obtain the correct steady-state gain for the speed controller. Since K_1 varies, the gain of the amplifier A is selected to make the product

$$AK_2 K_3 \cdot (K_1)_{\text{minimum}} \gg 1$$

The values of the time constants τ_1 and τ_3 are the remaining factors which determine system stability. Realistic values of τ_1 and τ_3 are:

$$\tau_1 = 0.001 \text{ sec} \quad \text{and} \quad \tau_3 = 0.005 \text{ sec}$$

Selecting a steady-state gain of 10 percent per hertz (typically, 12 1/2 percent per hertz has been used in previous power systems) and the other constants as mentioned above, the transfer function becomes

$$\frac{P(S)}{F(S)} = \frac{1.40(0.005S + 1)}{(0.005S + 1)(0.001S + 1) + 14}$$

This transfer function holds for small changes in speed. Further analysis reveals that the response of the power is a damped oscillation which dies out in about 0.008 sec. The response varies with changes in the value of K_1 . The response is increasingly oscillatory with increasing values of K_1 . A compensating network will be included in the final design to obtain a better response.

A SPEED-CONTROLLER DESIGN - Figure 10 is a block diagram of a new speed-controller design. Several characteristics not previously discussed are incorporated in this design. One characteristic is that only one of the multiple loads uses phase-controlled loading. Another is the provision for inhibiting the total-line-current limiters in case the alternator is required to produce more than its rated output power.

The amplified output of the frequency discriminator is fed to three summers - A1, A2, and A3. If the line current limiters are inactive, the full signal is provided to the level detectors and to summing junctions B1, B2, and B3. The outputs of these summing junctions are applied to the inputs of the isolation amplifiers. The magnitude of the phase-controlled load in resistors 1A, 1B, and 1C is linearly related to the output of the associated isolation amplifiers. Therefore, for the conditions specified, the load is directly proportional to the frequency deviation.

The level detectors for each phase are set to activate at equal increments of the frequency deviation. When a level detector turns on its associated load, a signal is provided by the conditioner and filter to reset the phase-controlled load to zero. This load transfer takes place for each multiple load in the speed controller. The resultant speed control characteristic is given in Fig. 11. The major nonlinearity is the small dead-band that will occur at each load transfer. The reason for using this scheme instead of multiple phase-controlled loads will be discussed later.

The function of the "cross-over detector" is to apply the fixed loads only when the line voltage goes through zero. This function enables the firing circuit to apply the load with a very small firing angle. Therefore, the line voltage distortion contributed by each of the multiple fixed loads is a minimum.

The line current regulator previously discussed provides a signal for the reduction of parasitic load current through summers C and A. The regulator override logic inhibits this

regulation if the frequency deviation is above some preselected value or if the alternator line current is greater than its rated value in each phase. The override function is required to prevent possible destructive high speeds when the system develops more than its rated power.

There are two major reasons for using only one phase-controlled load. The design and matching of firing circuits to obtain the same operating characteristics is much simpler when only three such circuits are used, and the phase-controlled load is allowed to have a high percentage unbalance between phases. This unbalance will not accumulate and raise the total alternator unbalance as would occur if multiple phase-controlled loads were used. A controller using six multiple loads requires 18 firing circuits. The remaining 15 firing circuits are readily matched since the load they control is either fully on or fully off. A disadvantage of this approach is the additional logic complexity required.

This new design incorporates ideas to improve the performance characteristics previously mentioned. The experimental limitations discussed by Perz are largely overcome by this design.

DIGITAL SPEED CONTROLLER

BASIC CHARACTERISTICS - The load sharing characteristic for the digital speed controller is given in Fig. 12. The characteristic is shown when, arbitrarily, 8 multiple loads are used over the normal control range. Arbitrary scales were selected for the ordinate and abscissa to facilitate the following discussion. Suppose that initially the useful load is equal to the alternator output power and that the frequency is at its rated value. When the useful load is decreased to 7.5, a power difference of 0.5 exists which increases the speed and electrical frequency of the alternator. The speed controller measures the frequency deviation. When the deviation exceeds 1.0, the controller applies a parasitic load of 1.0 after a certain delay time. This delay time is dependent on the design of the speed controller. Now an overload of 0.5 exists which decreases the frequency. The speed controller senses when the deviation is less than 1.0 and, after a delay time, removes the parasitic load. The load conditions are back to the starting point and the

cycle repeats. The frequency of the fluctuation is such that the time-average parasitic load is 0.5. When the useful load is reduced to 7.0, there will be no fluctuations if the parasitic load of 1.0 exactly complements the alternator output power. The above discussion applies equally to any load condition or frequency deviation. Exact load complements are difficult to achieve in this type of system; therefore, for all practical applications there will always be load fluctuations. The magnitude of the alternator load fluctuation is equal to the magnitude of the parasitic load step.

The waveshape of the parasitic load current for the fluctuating load is shown in Fig. 13. Each of the multiple loads conducts current for nearly the full 360 degrees of the sine wave or not at all. Computations have shown that firing angles of less than 1 degree can be obtained. The particular load that is fluctuating will conduct for an integral number of cycles. Since there is virtually no harmonic distortion of the parasitic load current, harmonic distortion of the line voltage is minimized. Some neutral current will flow until all three phases of the fluctuating load are turned on and again during turnoff. The loads are balanced to the degree that the parasitic load resistors are matched. The load balance is also a function of the balance of the line voltage. In addition, the absence of phase-controlled current implies that the apparent-power requirement of the alternator is not increased.

The load-frequency characteristic is now intentionally nonlinear. The resulting parasitic load fluctuations may cause undesirably large total alternator load and line voltage fluctuations. Therefore, the selection of an optimum parasitic load step is important. For example, preliminary calculations show that if 8 multiple loads were used in the 400-hertz Brayton system, the maximum voltage modulation would be about 3 percent. Maximum voltage modulation for systems employing phase-controlled loading is about 0.5 percent. The maximum frequency modulation with 8 multiple loads (for a 1 percent control range) would be about 0.06 percent. In present systems frequency modulation is about 0.01 percent.

A SPEED CONTROLLER DESIGN - A block diagram of a digital speed controller design is given in Fig. 14. The input to the sensing circuit is the line voltage. Its output is

a square wave with the same frequency as the input voltage. The frequency of this square wave is digitally compared with a constant frequency reference. The output of the comparator is a series of rectangular pulses. These pulses gate a high-frequency pulse generator. After a delay time determined by the period counter, the high-frequency pulses are sampled. The number of high-frequency pulses gated during the sampling interval is proportional to the deviation between the alternator frequency and the constant frequency reference. The counter stores this number. The decoder then determines the number of parasitic loads to be applied. Since the deviation can be positive or negative, the low frequency detector is used to prevent application of load below rated frequency.

PERFORMANCE REQUIREMENTS - A speed controller has been designed for a 400-hertz system using conventional integrated circuit logic. This design is capable of measuring frequency deviations of 0.0025 percent of rated frequency with a sampling period of 50 milliseconds; however, a final design must take into consideration the system in which it will be used.

System stability considerations determine the accuracy and the sampling period required of a speed controller. As was mentioned previously, the number of multiple parasitic loads that can be used is often fixed. Assume, for example, that 8 active loads are available for the 400-hertz Brayton system (9 kW net output rating). When each parasitic load step would be 1.12 kW (about 9 kW total for 8 steps). Therefore, the maximum power difference is 1.12 kW. For a rated power difference (9 kW) the acceleration rate of the turboalternator is about 1000 rpm/sec (this value can be calculated from information in Ref. 10). Assuming small speed changes, a 1.12 kW difference gives a rate of 125 rpm/sec. This rate is equivalent to a rate of about 4.2 Hz/sec. With a total control range of 4Hz, the frequency deviation between load steps is 0.5 Hz. For proper control of the speed, the controller must be able to measure deviations of less than 0.5 Hz and apply the proper loads before the deviation exceeds 0.5 Hz change. Therefore, the sampling period of the speed controller must not be greater than 0.12 sec. These performance limits for the speed controller appear feasible.

CONCLUDING REMARKS

Improvement in the electrical performance characteristics of space power systems can be obtained by modifying present speed controller designs or by using an all-digital design. The selection of a design depends upon limitations of the system in which it will be used. An important limitation is the number of parasitic load resistors that can be used.

For example, if the number of multiple loads must be small (say 4 to 8) and if the voltage and frequency modulation must be kept to a minimum, then the phase-controlled loading speed controller would be selected. But, if the number of multiple loads can be large (say 32), then the digital speed controller would be selected. The advantages of the digital speed controller are:

1. There is no additional volt-ampere requirement on the alternator.
 2. The distortion of the line voltage is at a minimum.
 3. The neutral current is essentially zero.
 4. The parasitic load has a minimum unbalance.
 5. The quasilinear control characteristic can be quite accurate with high repeatability.
- With a large number of multiple loads, the voltage and frequency modulation inherent in the digital speed controller can approach the values obtained with the phase-controlled method.

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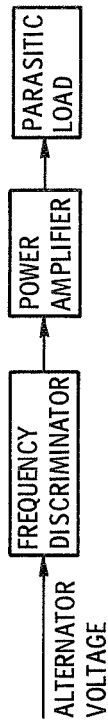
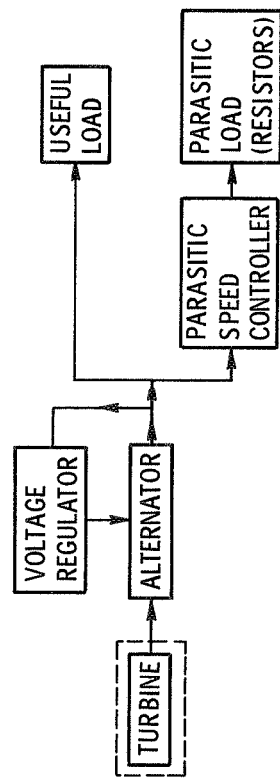
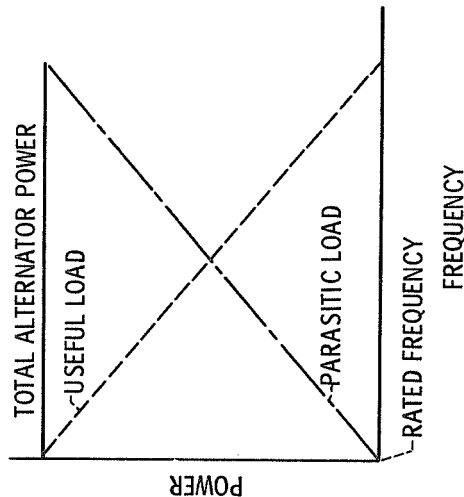


Figure 2. - Block diagram of parasitic loading speed controller.



(A) BLOCK DIAGRAM OF THE ELECTRICAL SYSTEM.



(B) IDEAL LOAD DIVISION OF THE ALTERNATOR.

Figure 1

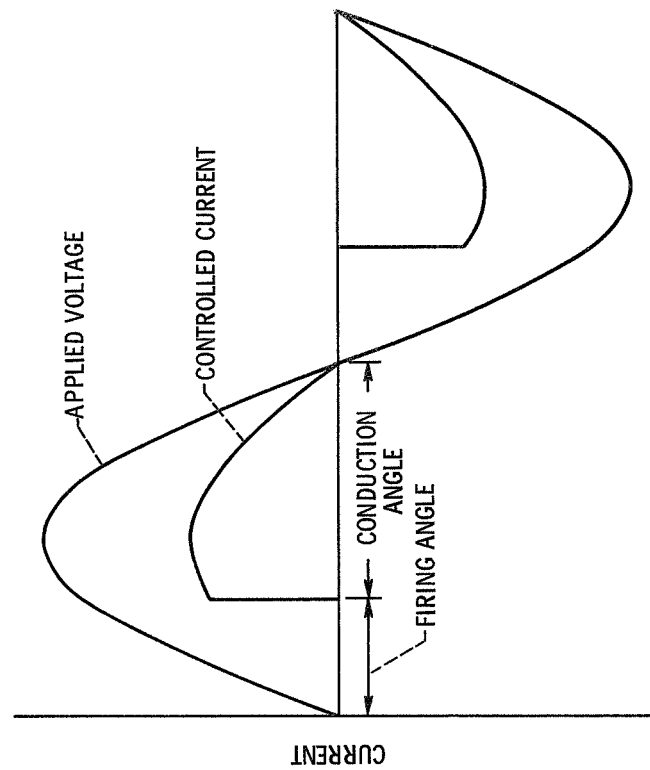


Figure 3. - Waveshape of phase-controlled current.

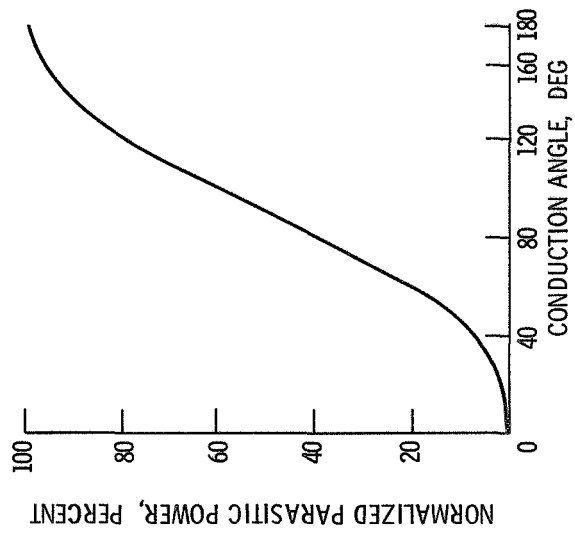


Figure 4. - Normalized parasitic power as a function of SCR conduction angle.

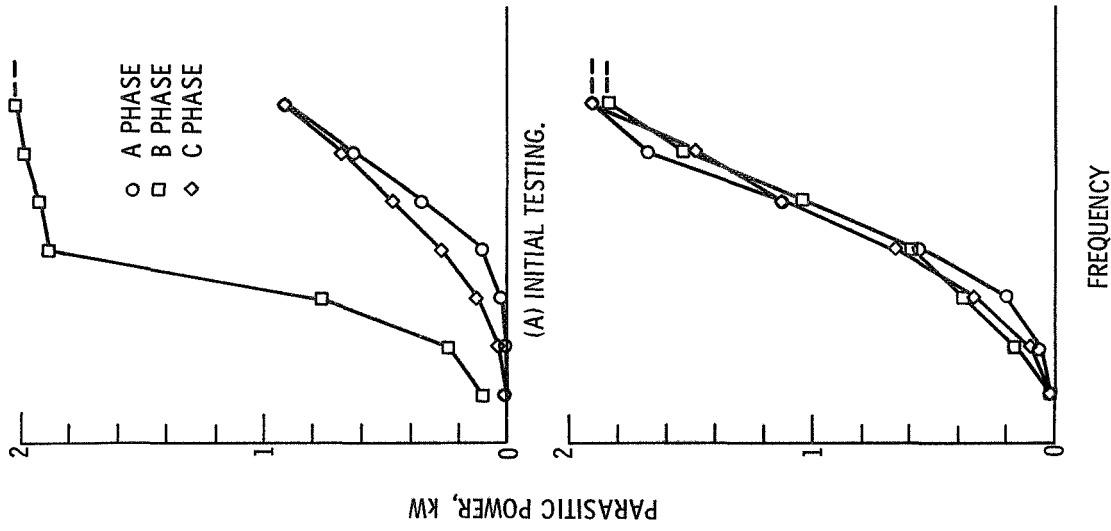


Figure 5. - Control characteristics of 1200-hertz Brayton speed controller.

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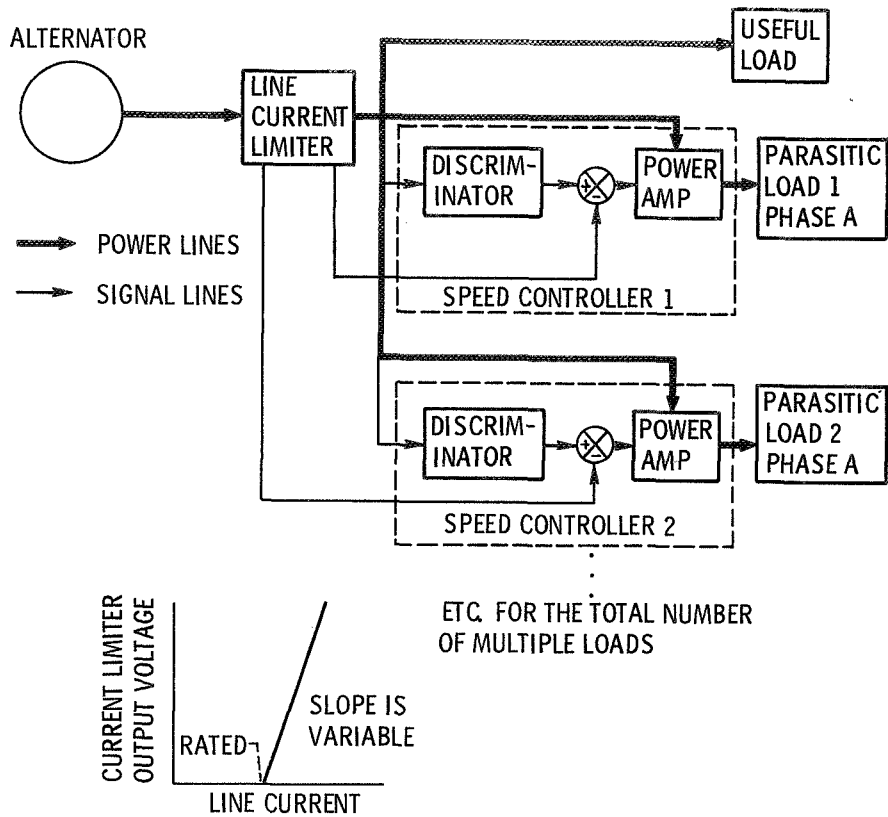
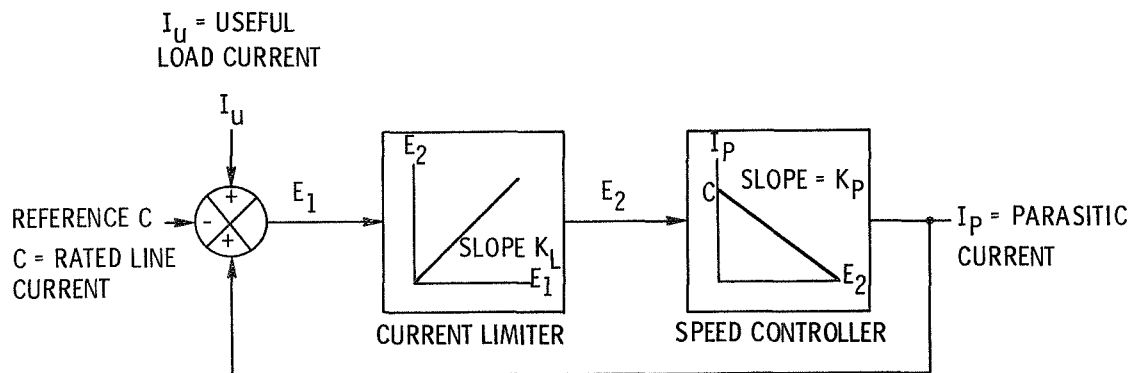
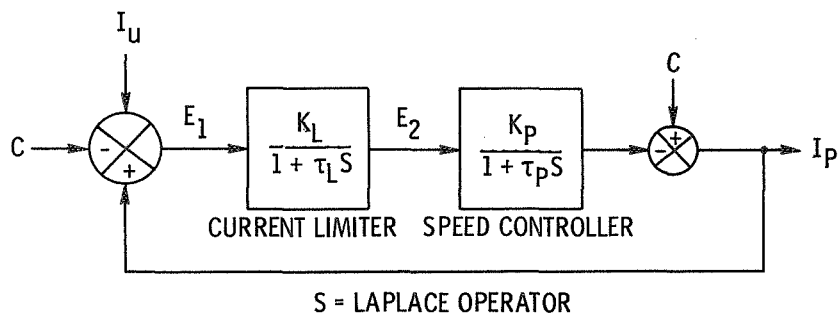


Figure 6. - Line diagram of current limiting for one phase of the alternator output.



(A) FUNCTIONAL BLOCK DIAGRAM OF CURRENT LIMITING METHOD.



(B) BLOCK DIAGRAM OF LIMITER IN TERMS OF TRANSFER FUNCTIONS.

Figure 7

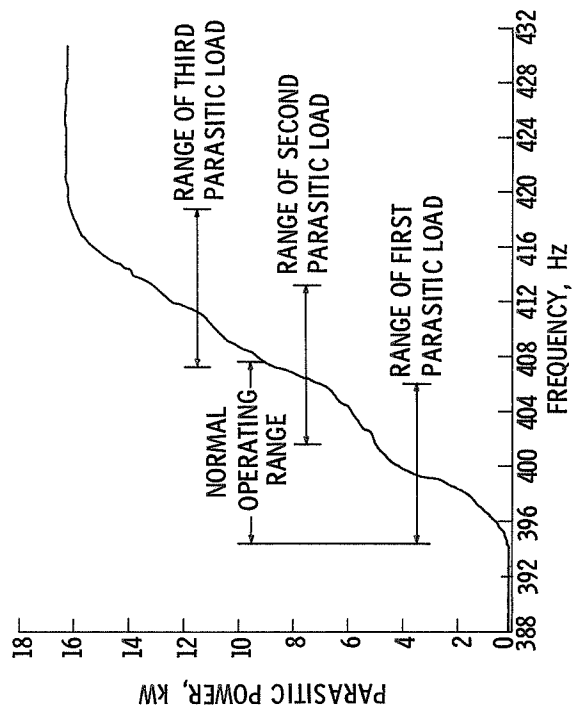


Figure 8. - Experimental speed-controller characteristic for the 400-hertz Brayton system (curve obtained from ref. 2).

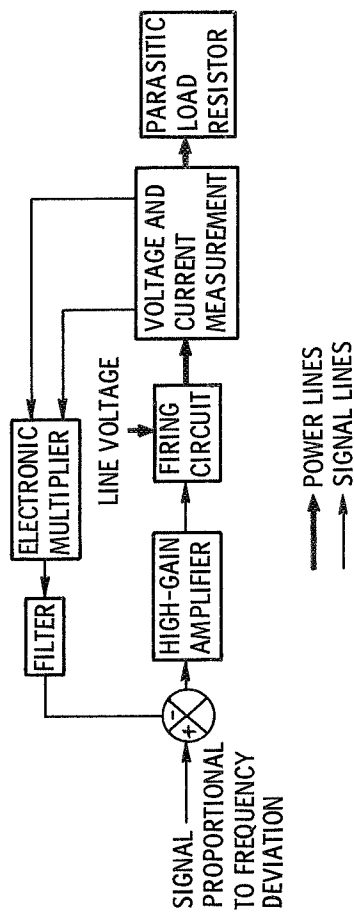
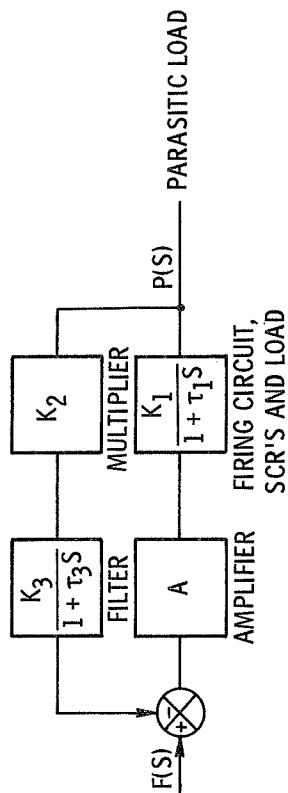


Figure 9(a). - Block diagram of method to linearize the load-frequency characteristic.



$S = \text{LAPLACE OPERATOR}$

THE AMPLIFIER AND THE MULTIPLIER ARE CONSIDERED TO HAVE NO TIME DELAY.

Figure 9(b). - Block diagram in terms of Laplace transforms.

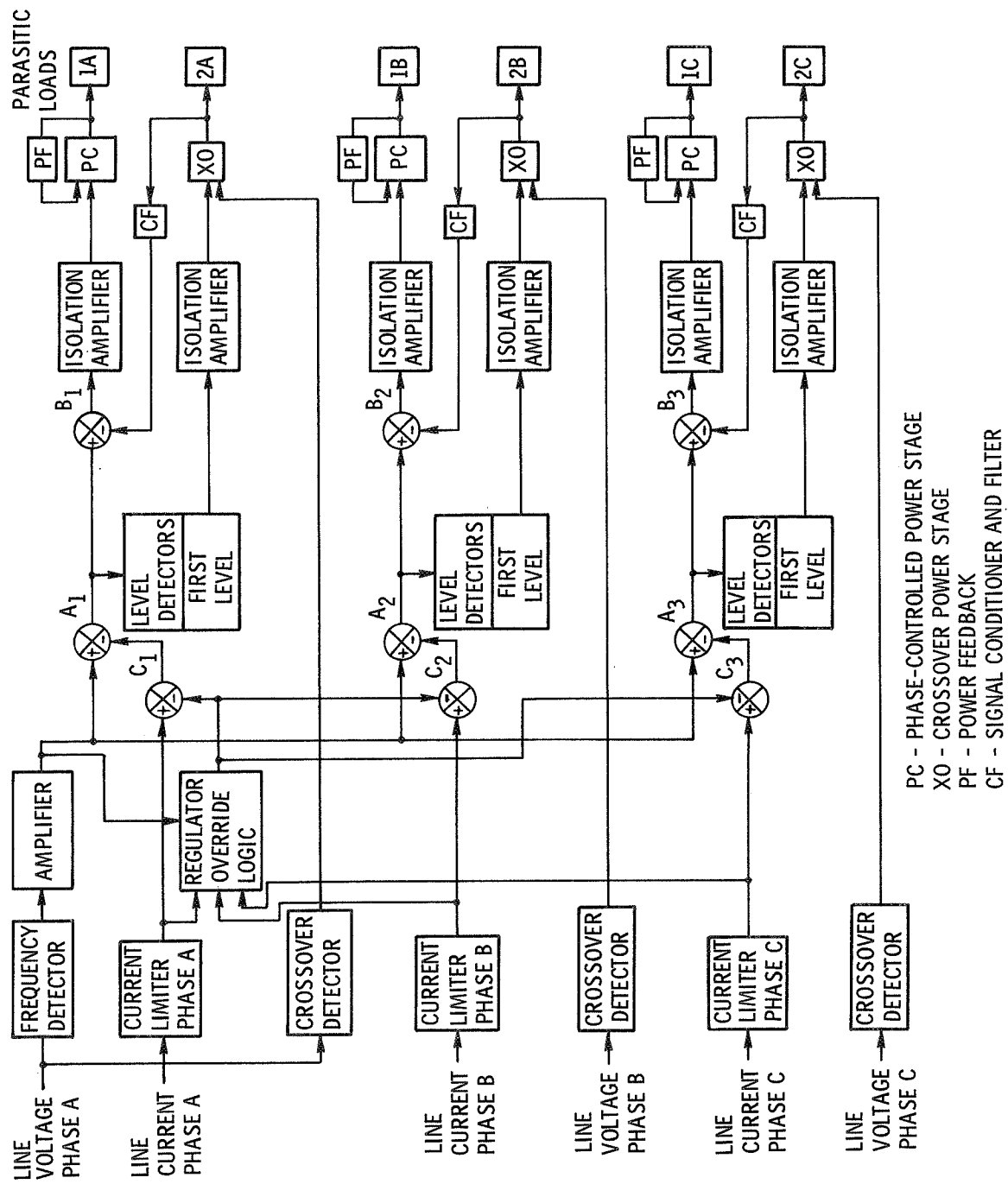


Figure 10. - Block diagram of the phase-controlled speed controller.

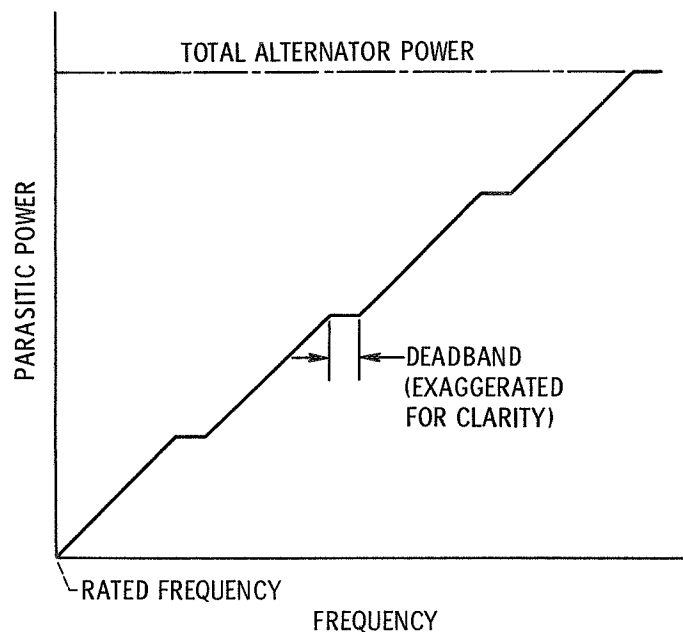


Figure 11. - Control characteristic of speed controller when one phase-controlled load is used.

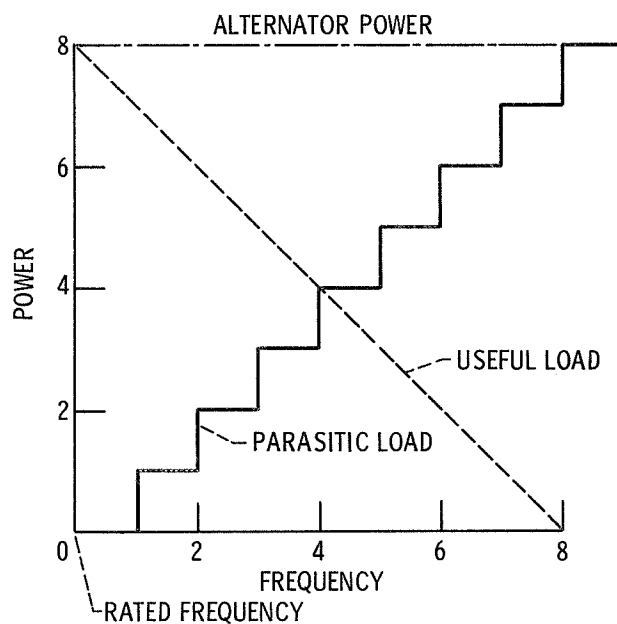


Figure 12. - Load sharing for the digital speed controller.

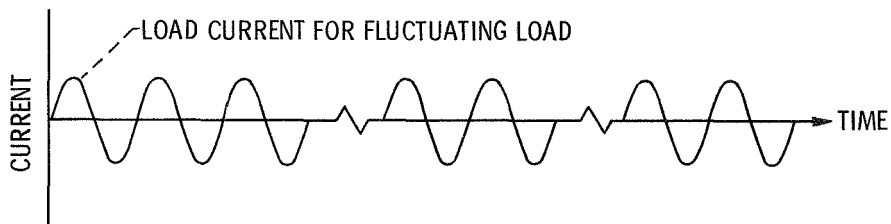


Figure 13. - Parasitic current waveshape for the digital speed controller.

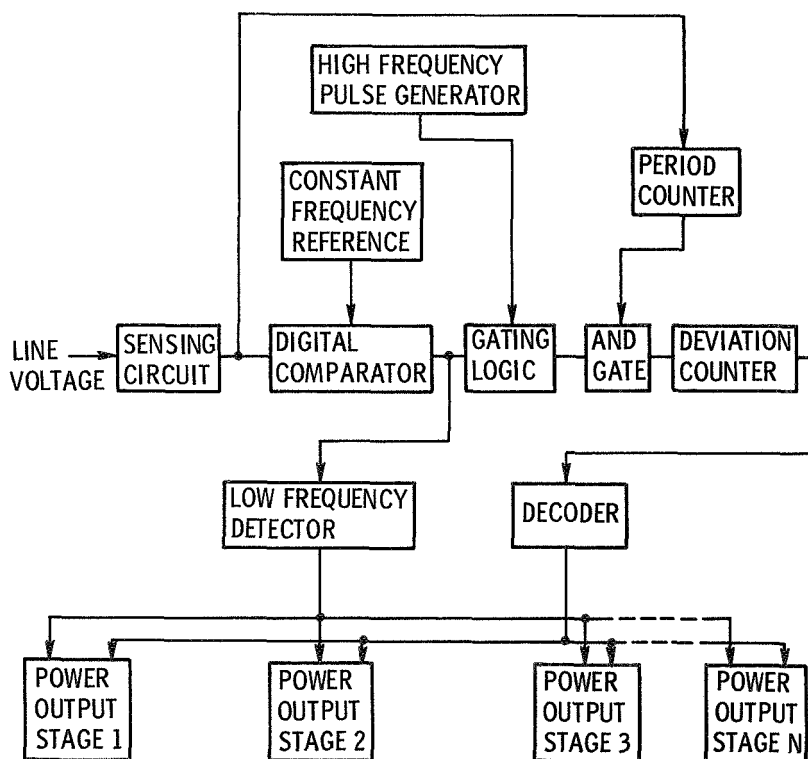


Figure 14. - Block diagram of the digital speed controller.